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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tzartzanis, et al.

Serial No.: 10/779,464

Filed: February 13, 2004

For: DIFFERENTIAL CURRENT-
MODE SENSING METHODS
AND APPARATUSES FOR
MEMORIES

Art Unit: 2818

Examiner: Unknown

Atty. Dkt.: 02EK-108868

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MAILING/TRANSMISSION
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PURSUANT TO 37 C.F.R. §1.56 AND §§1.97-1.98**

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Sir:

The citations listed on the enclosed PTO-1449 Form are submitted under 37 C.F.R.
§§1.97 and 1.98, and in compliance with the duty of disclosure as defined in 37 C.F.R. §1.56.

The Examiner is requested to make these citations officially of record in the application.
This Information Disclosure Statement is being submitted before receipt of the first Office
Action for the above-identified application, therefore, pursuant to 37 C.F.R. §1.97, no fee or
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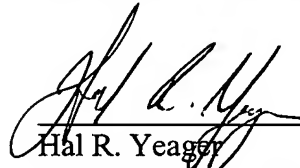
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claim in the above-identified application. Additionally, this Information Disclosure Statement is

not to be construed as a representation that a further search of the art has been made by Applicants, or that additional information relevant to the examination of this application does not exist unbeknownst to Applicants.

Date: June 17, 2004

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Respectfully submitted,



Hal R. Yeager
Registration No. 35,419



FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 02EK-108868	SERIAL NO. 10/779,464
	APPLICANT Tzartzanis, et al.	
	FILING DATE: February 13, 2004	GROUP ART UNIT: 2818

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAM'R INITIAL		DOCUMENT NUMBER	DATE	NAME	Class	Subclass	Filing Date If Appropriate
	A						
	A						
	A						

FOREIGN PATENT DOCUMENTS

EXAM'R INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	Subclass	TRANSLAT'N	
							yes	no
	B							
	B							

OTHER ART (Include Author, Title, Date, Pertinent Pages, Etc.)

	C1	R. Foss, R. Harland, "Peripheral Circuits for One-Transistor Cell MOS RAM's", IEEE Journal of Solid-State Circuits, Vol. SC-10, No. 5, October 1975.
	C2	N. Lu, H. Chao, "Half-V _{dd} Bit-Line Sensing Scheme in CMOS DRAM's" IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984.
	C3	S. Dhong, N. Lu, W. Hwang, S. Parke, "High-Speed Sensing Scheme for CMOS DRAM's", IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, February 1988.
	C4	S. Shinagawa, et al., "A Multi-Speed Digital Cross-Connect Switching VLSI Using New Circuit Techniques in Dual Port RAMs," IEEE Custom-Integrated Circuits Conference, 1991.
	C5	T. Blalock, R. Jaeger, "A High-Speed Clamped Bit-Line Current-Mode Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991.
	C6	Seevinck, P. van Beers, H. Ontrop, "Current-Mode Techniques for High-Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAM's," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991.
	C7	T. Blalock, R. Jaeger, "A High-Speed Sensing Scheme for IT Dynamic RAM's Utilizing the Clamped Bit-Line Sense Amplifier," IEEE Journal of Solid-State Circuits; Vol. 27, No. 4, April 1992.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant(s).

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	C8	M. Izumikawa, M. Yamashina, "A Current Direction Sense Technique for Multiport SRAM's," IEEE Journal of Solid-State Circuits, Vol. 31, No. 4, April 1996.
	C9	N. Tzartzanis, W. Athas, "Clock-Powered Logic for a 50MHz Low-Power RISC Datapath," IEEE ISSCC Digest of Technical Papers, pp. 338-339, San Francisco, CA, Feb. 6-8, 1997.
	C10	W. Athas, et al., "A Low-Power Microprocessor Based on Resonant Energy," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997.
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	C12	W. Athas, et al., "WA 17.5 Clock-Powered CMOS VLSI Graphics Processor for Embedded Display Controller Application," IEEE International Solid-State Circuits Conf., February 2000.
	C13	N. Tzartzanis, W. Athas, L. Svensson, "A Low-Power SRAM with Resonantly Powered Data, Address, Word, and Bit Lines," Proceedings of the 2000 European Solid-State Circuits Conference (ESSCIRC'2000), Sept. 19-21, 2000, Stockholm, pp. 336-339.
	C14	Y. Takao, et al., "A 0.1µm CMOS Technology with Copper and Very-low-k Interconnects for High-Performance System-On-a Chip Cores," International Electron Devices Meeting, pp. 559-562, San Francisco, CA, October 10-13, 2000.

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	C15	W. Athas, et al., "The Design and Implementation of a Low-Power Clock-Powered Microprocessor," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, Nov. 2000.
	C16	N. Tzartzanis, W. Walker, H. Nguyen, A. Inoue, "A 34 Word 64 Bit 10R/6W Write-Through Self-Timed Dual-Supply-Voltage Register File," ISSCC Digest of Technical Papers, San Francisco, CA, February 4-6, 2002.
	C17	R. Riedlinger, T. Grutkowski, "The High-Bandwidth 256kB 2nd Level Cache on an Itanium Microprocessor," ISSCC Digest of Technical Papers, San Francisco, CA, February 4-6, 2002.
	C18	D. Bradley, P. Mahoney, B. Stackhouse, "The 16kB Single-Cycle Read Access Cache on a Next-Generation 64b Itanium Microprocessor," IEEE ISSCC Digest of Technical Papers, San Francisco, CA, February 4-6, 2002.
	C19	S. Tang, et al., "A Leakage-Tolerant Dynamic Register File Using Leakage Bypass with Stack Forcing (LBFS) and Source Follower NMOS (SFN) Techniques," Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, HI, June 13-15, 2002.
	C20	S. Hsu, et al., "A 90nm 6.5GHz 256x64b Dual Supply Register File with Split Decoder Scheme", Symposium on VLSI Circuits, June 2003.

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